What is claimed is:

1. A nonvolatile semiconductor memory device comprising:

a memory cell array in which a plurality of memory cells are arranged in a row direction and a column direction,

wherein the memory cell array includes a plurality of element isolation regions,

wherein each of the memory cells includes a first impurity layer, a second impurity layer, a channel region located between the first impurity layer and the second impurity layer, a word gate and a select gate disposed to face the channel region, and a nonvolatile memory element formed between the word gate and the channel region, and

wherein a first wordline connection section, which connects at least one of a plurality of word gate interconnects with at least one of the word gates, is disposed over at least one of the element isolation regions.

2. The nonvolatile semiconductor memory device as defined in claim 1,

wherein the memory cell array includes a plurality of memory blocks,

wherein each of the memory blocks includes the memory cells, and

wherein an operation of erasing data held in each of the memory cells is performed at the same time for each of the memory blocks.

3. The nonvolatile semiconductor memory device as defined in claim 1,

wherein the memory cells includes a plurality of word-gate rows, each of the word-gate rows is formed by connecting the word gates in the memory cells arranged in the row direction, and

wherein the nonvolatile semiconductor memory device further includes a plurality of common connection sections, each of the common connection sections connecting two of the word-gate rows adjacent in the column direction over one of the

element isolation regions on which the first wordline connection section is disposed.

4. The nonvolatile semiconductor memory device as defined in claim 3,

wherein the first wordline connection section connects at least one of the word gate interconnects with one of the common connection sections.

5. The nonvolatile semiconductor memory device as defined in claim 2,

wherein the memory cells includes a plurality of word-gate rows, each of the word-gate rows is formed by connecting the word gates in the memory cells arranged in the row direction,

wherein the nonvolatile semiconductor memory device further includes a plurality of common connection sections, each of the common connection sections connecting two of the word-gate rows adjacent in the column direction over one of the element isolation regions on which the first wordline connection section is disposed, and

wherein each of the word gates in the memory block is connected with all of the word gate interconnects in the memory block.

6. The nonvolatile semiconductor memory device as defined in claim 3,

wherein each of the word gate interconnects includes a first interconnect extending along the row direction, and a second interconnect extending along the column direction, and

wherein a second wordline connection section, which connects one of the common connection sections with the second interconnect, is disposed over at least one of the element isolation regions.

7. The nonvolatile semiconductor memory device as defined in claim 6,

wherein the first wordline connection section includes the second wordline

connection section.

8. The nonvolatile semiconductor memory device as defined in claim 5,

wherein each of the word gate interconnects includes a first interconnect extending along the row direction, and a second interconnect extending along the column direction, and

wherein a second wordline connection section, which connects one of the common connection sections with the second interconnect, is disposed over at least one of the element isolation regions.

9. The nonvolatile semiconductor memory device as defined in claim 8,

wherein the first wordline connection section includes the second wordline connection section.

10. The nonvolatile semiconductor memory device as defined in claim 1,

wherein the memory cell array includes at least one source interconnect and a plurality of first source line connection sections, and

wherein each of the first source line connection sections connects the source interconnect with the first impurity layer.

11. The nonvolatile semiconductor memory device as defined in claim 10,

wherein the source interconnects include a third interconnect extending along the row direction, and a fourth interconnect extending along the column direction, and

wherein at least one of the first source line connection sections includes a second source line connection section which connects the third interconnect with the fourth interconnect.

12. The nonvolatile semiconductor memory device as defined in claim 1,

wherein the memory cell array includes at least one source interconnect and a plurality of first source line connection sections, and

wherein each of the first source line connection sections connects the source interconnect with the second impurity layer.

13. The nonvolatile semiconductor memory device as defined in claim 12,

wherein the source interconnects include a third interconnect extending along the row direction, and a fourth interconnect extending along the column direction, and

wherein at least one of the first source line connection sections includes a second source line connection section which connects the third interconnect with the fourth interconnect.